UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,054,774 B2
APPLICATION NO. : 10/609329
DATED : May 30, 2006
INVENTOR(S) : Batterberry et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title page, Item (56), under "Other Publications", in column 2, line 2, delete "Mu**tlit**media" and insert -- Mu**lti**media --, therefor.

On Title page 2, Item (56), under "Other Publications", in column 2, line 16, delete "Join**g**" and insert -- Join**t** --, therefor.

On Title page 2, Item (56), under "Other Publications", in column 2, line 18, delete "page**r**" and insert -- page**s** --, therefor.

On Title page 2, Item (56), under "Other Publications", in column 2, line 40, delete "**iv**deo" and insert -- **vi**deo --, therefor.

On Title page 2, Item (56), under "Other Publications", in column 2, line 41, delete "Network**ign**" and insert -- Network**ing** --, therefor.

In column 7, line 54, after "extended" delete "n" and insert -- **i**n --, therefor.

In column 12, line 9, after "method" delete "11".

In column 14, lines 25–41, delete "As shown in FIG. 7, the computing environment 920 includes a general-purpose computing device in the form of a computer 930. The components of computer 920 may include, by are not limited to, one or more processors or processing units 932, a system memory 934, and a bus 936 that couples various system components including the system memory 934 to the **processor 932. Bus 936 represents** one or more of any of several types of bus structures, including a memory bus or memory controller, a peripheral bus, an accelerated graphics port, and a processor or local bus using any of a variety of bus architectures. By way of example, and not limitation, such architectures include Industry Standard Architecture (ISA) bus, Micro Channel Architecture (MCA) bus, Enhanced ISA (EISA) bus, Video Electronics Standards Association (VESA) local bus, and Peripheral Component Interconnects (PCI) buss also known as Mezzanine bus." and insert
-- As shown in FIG. 7, the computing environment 920 includes a general-purpose computing device in the form of a computer 930. The components of computer 920 may include, by are not limited to, one or more processors or processing units 932, a system memory 934, and a bus 936 that couples various system components including the system memory 934 to the **processor 932.**

Bus 936 represents one or more of any of several types of bus structures, including a memory bus or memory controller, a peripheral bus, an accelerated graphics port, and a processor or local bus using any of a variety of bus architectures. By way of example, and not limitation, such architectures include Industry Standard Architecture (ISA) bus, Micro Channel Architecture (MCA) bus, Enhanced ISA (EISA) bus, Video Electronics Standards Association (VESA) local bus, and Peripheral Component Interconnects (PCI) buss also known as Mezzanine bus. --, therefor.

In column 17, line 14, in Claim 1, delete "sewer" and insert -- server --, therefor.

In column 17, line 29, in Claim 1, delete "sewer" and insert -- server --, therefor.

Signed and Sealed this

Thirteenth Day of April, 2010

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office